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"Performance degradation of downscaled SoCs due to crosstalk from digital to analog", pp.258 - 271

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Abstract – In the last decades, scaling according to Moore's law has led to increased performance and complexity of systems on chip (SoCs). This scaling will continue, enabling the development of the world of ambient intelligence, in which complex mixed-signal ICs, supported with sensors and actuators will play a key role. However, the committees of the International Technology Roadmap for Semiconductor Technology (ITRS) that develop the schedule for CMOS scaling foresee problems with the integration of analog functions. The major problem is a poor signal isolation between the digital and the analog parts of a chip, causing crosstalk from digital to analog. This crosstalk mainly happens via the semiconducting silicon substrate, which is usually treated as a ground node by analog and RF designers. The substrate noise coupling problem leads more and more to malfunctioning or extra design iterations. One of the reasons is that the phenomenon of substrate noise coupling is difficult to model and hence difficult to understand. It can be caused by the switching of thousands or millions of gates and it can depend on layout details. From the generation side (the digital domain), coping with the large amount of noise generators can be solved by macromodeling. On the other hand, the impact of substrate noise on the analog circuits requires careful modeling at the level of transistors and parasitics of layout, power supply, package, PCB… Comparison to measurements of macromodeling at the digital side and careful modeling at the analog side, shows that both the generation and the impact of substrate noise can be predicted with an accuracy of a few dB. In addition, this combination of macromodeling at the digital side and careful modeling at the analog side leads to an understanding of the problem, which can be used for digital low-noise design techniques to minimize the generation of noise, and substrate noise immune design of analog/RF circuits. In addition to the crosstalk problem, the degradation of the analog performance of a transistor, can lead to lower circuit performance. We show in this paper, both with simulations and with fabricated designs in 90 nm, that the speed improvement dominates the analog performance degradation for typical analog and RF circuits that are used in telecom applications. In this way, circuit performance improves or power consumption can be lowered for a given performance.