

“A low noise fractional-N approach with a short periodicity of the division factor sequences”,
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Abstract – High-end measurement systems often rely on frequency synthesisers with an extremely low phase noise level. A fractional-N PLL-concept with an excellent phase noise performance together with a moderate frequency resolution is presented. The fractional-N concept is mainly based on fully digital approaches, however, the length of the division factor sequences is strictly limited to allow for a filtering of the spurious signals in the loop filter. The functionality of the concept is demonstrated in a prototype system based on a single phase locked loop (PLL). The presented synthesiser shows a phase noise level below -109.8 dBc/Hz at a carrier offset frequency of 5 kHz for a microwave signal at 8 GHz. The frequency step width of the synthesiser is 9.72MHz with a reference frequency of the crystal oscillator of 155.52 MHz. The different components of the system like a broadband VCO and the fractional PLL are addressed in this article. The VCO exhibits a tuning range of 4 GHz up to 11 GHz with a free running phase noise level in the order of -100 dBc/Hz at a carrier offset of 200 kHz. Thus, the PLL has to improve the phase noise close to the carrier considerably. This is possible with a high filter bandwidth of the PLL loop filter. The necessary loop bandwidth results in a frequency resolution of the PLL of 9.72 MHz. Compared to a fully digitally compensated fractional-N PLL the set-up is not able to perform arbitrarily fine frequency steps, but it allows for an optimized phase noise level. However, if further improvements in the frequency resolution are required, this concept can easily be combined with other synthesiser techniques like multiple loop structures.