A Behavioral Model for a Wideband RF Analog-to-Digital Converter

John Wood[1], Matt Straayer[2]
[1]Maxim Integrated, Inc, San Jose, CA USA
email: john.wood@ieee.org
[2]Maxim Integrated, Inc, Chelmsford, MA USA

***Abstract*—We describe a behavioral model of an interleaving RF-to-digital ADC. The ADC has an input bandwidth of over 3 GHz, and is a 16-bit interleaved digitizer. The model includes both analog and digital parts, describing the analog nonlinearity and frequency response, and digital impairments such as jitter, thermal noise, and interleaving errors. The model is implemented in a commercial simulator. The model is built from simulated data to enable the design of RF system architecture prior to the availability of first silicon.**

I. Introduction

Recent commercial developments of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) that operate directly between the digital domain and radio frequencies (RF), and offer wide instantaneous bandwidth, are about to enable the promise of software-defined radio architectures in practical applications such as wireless infrastructure transmitters. These data converters offer considerable advantages in simplifying transceiver systems, for example, by eliminating the impairments and distortions associated with analog modulators and demodulators, such as IQ imbalance and local oscillator phase noise by moving these functions into the digital domain, and also by enabling multi-band signal transmission due to their extremely wide bandwidth. An example schematic of a transmitter linearized by digital pre-distortion (DPD), and using RF-DAC and RF-ADC components is shown in Fig. 1, illustrating the simplicity of the RF domain.

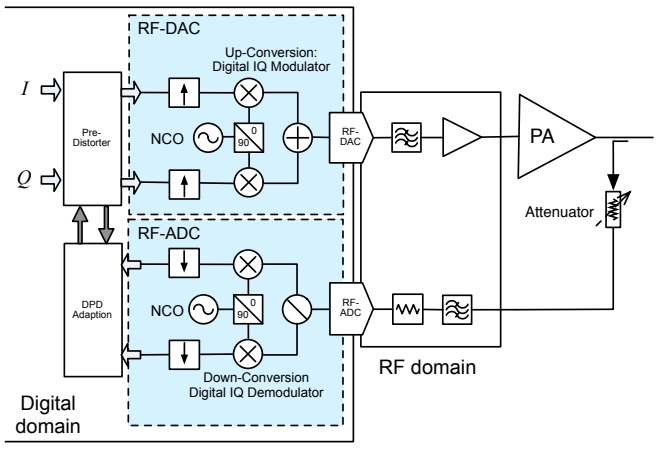

Fig. 1. A transmitter with digital pre-distortion linearization using RF-DAC and RF-ADC components to simplify the analog paths.

While the architecture of this system appears simple, it is nevertheless important to be able model the complete system to ensure that the individual components work together and allow the overall system specifications to be met. This means that we need accurate models for each of the components in the system. These models are typically behavioral models that are used in the system-level design to validate the chosen architectural approach.

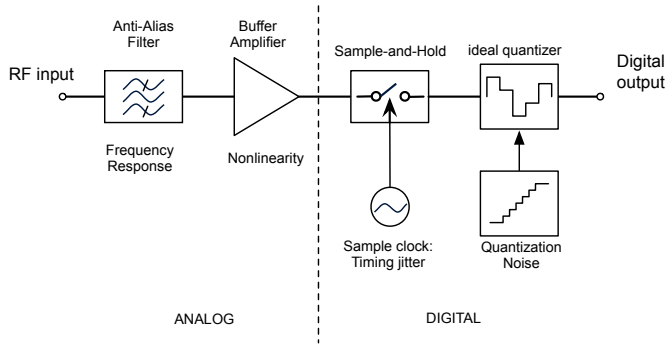

Fig. 2. Classic model structure for an ADC.

The classic ADC model structure is shown in Fig. 2, illustrating the analog and digital aspects. While commercial ADC manufacturers generally provide models for their products, these are usually simplified analog/digital designs that are targeted at the lower-frequency products (see, for example [1]. For higher-frequency ADCs, the RF behavior is often described using an S-parameter block for the front end: a linear model.

Several nonlinear models of ADCs can be found in the literature. Vogel and Koeppl [2] describe a nonlinear behavioral model of an interleaving ADC using Mathworks MATLAB®. While this model uses a normalized frequency description, it is essentially a low-frequency ADC. A model for a 500 MS/s multistage ADC has been reported [3], using standard Mathworks Simulink® blocks, for use in digital simulation. Analog nonlinearities in ADCs have been modeled successfully using a Volterra series approach [4]. A good review of the state of the art in ADC modeling is presented by Arpaia [5]. Most of the reported ADC modeling does not address direct RF-to-digital converters.

In this paper, we describe the construction of a nonlinear behavioral model of an interleaving RF-ADC that can be used as a direct RF-to-digital receiver. The ADC has an input bandwidth of over 3 GHz, and is a 16-bit interleaved digitizer. The model captures the analog nonlinearity and frequency response in the RF domain and includes digital impairments such as jitter, thermal noise, and interleaving errors. The model is constructed in MATLAB and designed to run in RF system

simulators such as Keysight 'Ptolemy'® and AWR 'VSS'®: this latter simulator is used for the examples in this paper. The model is built from data obtained from circuit simulations, and its purpose is to allow accurate and meaningful RF system-level design to begin before the ADC is available in silicon, enabling customers to validate their system design before the product is available, resulting in faster time-to-market.

II. ADC Model Structure and Simulator Constraints

We use the ADC model structure shown in Fig. 2. The ADC analog input is a wideband buffer amplifier and anti-alias filter, and the model for these parts includes frequency response and any nonlinearity and memory effects associated with this buffer amplifier. To the digital function of the ADC – the sampling and quantization – are added jitter and quantization noise effects, and interleaving artifacts.

In the digital systems domain, MATLAB and Simulink are popular simulator choices. In the RF domain, we prefer frequency domain simulators such as Harmonic Balance, as found in Keysight 'ADS'® and AWR 'Microwave Office'® simulators. To simulate the linearized transmitter in Fig. 1, we need to accommodate the digital and RF domains, and the data converter models must function in both domains. The system simulation is performed using a discrete-time simulator operating on complex envelope baseband signals at a fixed sample rate that is sufficient to capture the 3-5 times instantaneous bandwidth of the signal required for digital pre-distortion (DPD). We use Ptolemy or VSS for these simulations. In these time-stepping simulators, an accurate representation of the anti-alias filter response and the nonlinear behavior of the buffer amplifier require considerable further over-sampling of the data rate.

Generally, the data rate will not be the same as the ADC sample (clock) rate, and this must be accommodated in the design of the model. The baseband data is in the form $I + jQ$, whereas the RF-ADC operates on a real (RF) data input. We have to change the data from complex baseband to real RF representation before we input to the ADC model. These, and other model–simulator considerations, are outlined in the detailed model description below.

III. Analog Front End

The filter+nonlinearity structure for the analog part of the ADC shown in Fig. 2 is the Wiener model structure, which is a simplified Volterra Model. While the Volterra approach has been used successfully to model ADCs [4], here we use an alternative simplified model: the Hammerstein model structure, where the filter follows the nonlinearity. This has no effect on the model performance, but makes the identification of the model parameters using least-squares techniques much simpler. The filter is not an anti-alias filter in the traditional sense, but a wideband low-pass filter defining the analog input bandwidth.

As noted earlier, to get an accurate representation of the filter characteristics in the system simulator, we need to over-sample the input complex data significantly. The oversampling rate (OSR) can be five to ten times the data rate to get a good description of the impulse response of the filter. Given that the ADC sampling rate is about 3 GHz, the oversampled data rate was chosen to be around 24 GHz; the actual value is an integer multiple of the data sampling rate, since a multi-rate filter was used to interpolate the input baseband signal to the oversampled data rate. This oversampled complex baseband data is then converted to real data at the RF carrier frequency of interest, using the well-known transform:

$$x(t) = I(t)\sqrt{2}\cos(\omega_c t) - Q(t)\sqrt{2}\sin(\omega_c t) \qquad (1)$$

where $I(t)$ and $Q(t)$ are the in-phase and quadrature components of the complex baseband signal, and ω_c is the RF carrier frequency.

The data for the analog front end was obtained from circuit-level simulation over the frequency range from 0.5 to 4 GHz, using two-tone signals at -1 dBFS total signal level. The buffer amplifier is designed to be as linear as possible, and the wideband low-pass filter frequency response in the passband is designed to be as flat as possible for the ADC application. The Hammerstein model was identified from this wideband input-output data, using QR factorization. The model is a mild cubic nonlinearity and FIR filter with 20 taps. The model fit to the simulated data is shown in Fig. 3; NMSE is better than -50 dB.

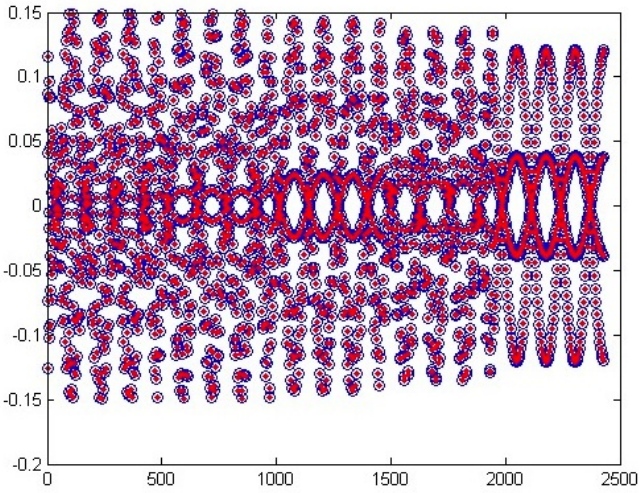

Fig. 3. Time-domain voltage data *versus* sample number for the Hammerstein model fit (red) to simulated data (blue) for the analog front end.

IV. Sampler and Digitizer model

The output of the analog front end model is a real signal that is oversampled at around 24 GHz. This signal is then decimated to the ADC sample rate, about 3 GHz. Again, the precise value of the sampling rate depends on the oversampling rate and the integer decimation. Circuit simulation indicates that the voltage at the instant of sampling is sufficient to describe the voltage passed to the quantizer: the sampling and hold operations do not introduce any artifacts into the signal.

The derivative of the oversampled signal is also determined, using a differentiating filter, and this is then also decimated to the ADC sample rate using a multi-rate filter. This gives us the slope of the voltage at the sample instants; by multiplying this slope by the sampling jitter, δt, then the sampled voltage

error due to the sample timing error can be estimated and built into the model.

The ADC digitizer consists of N interleaved ADCs. This was modeled by taking N consecutive samples of the decimated data, and applying a 16-bit digitizer on each of the samples. In each digitizer, we can add the following impairments to this sampled voltage:

- Thermal noise voltage;
- Offset error voltage;
- Error voltage arising from the timing error in the sampling instant. The sample timing error comprises a timing offset or skew, and the sample-to-sample jitter.

The offset error voltages and timing skew are determined by taking a normally-distributed random value over the nominal range of expected values from the IC process and the circuit layout. The range of values is obtained from Monte Carlo simulation. This yields different values of these impairments for each of the digitizers; these values are fixed for the duration of the simulation. While the values are randomly chosen, the randomize seed is fixed so that the results are repeatable between simulations, for consistency and validation of the model. The timing jitter is also estimated in this way, but is recalculated for each sample in the N samples, for every set of N samples. The range of values for the various impairments is consistent with the expected mismatch of the interleaved channels.

The quantized output at the ADC sample rate, including the quantization and interleaving errors outlined earlier, is then converted back to a complex envelope signal, and decimated to the baseband data rate using a multi-rate lowpass filter. We can then compare directly the input and output complex-modulated signals in the system simulator.

V. Model Implementation

The model is constructed in Mathworks MATLAB, in modular form. The Digital Signal Processing Toolbox was used for the generation of the multi-rate filters for interpolation and decimation, and for the differentiating filter used for the jitter estimation. The MATLAB model can then be ported easily to the target system simulators, VSS and Ptolemy, which have straightforward interfaces for implementing MATLAB functions in the schematic window, without major changes to the model structure.

VI. Model Performance

Each module of the model was tested independently, and then cascaded. For testing the analog blocks and back-end conversion back to complex envelope, single- and two-tone signals were used. Continuity of the signal across data block boundaries was ensured by the multi-rate filters, and their operation verified using two-tone signals and comparing with analytic calculations. The accuracy of the derivative filter was also verified against analytic calculation of the derivative. The digital sampling and digitizing blocks were checked for monotonicity, with and without noise added.

Once we were satisfied with the functionality of the model in MATLAB, the model was introduced into a simple VSS test circuit, using single-tone and digital modulated signals for testing and observing the model output on a spectrum analyzer instance. The resolution bandwidth of the spectrum analyzer is set to 30 kHz. The digital impairments were added individually and their effects observed at the output of the digitizer module.

Using single-tone testing, the interleaving errors produced by including all the impairments apart from thermal noise were found to be below -115 dBc. Adding thermal noise, the noise floor is close to the value measured on first silicon, with some spurs visible yielding a spurious-free dynamic range (SFDR) of 82.5 dB. This compares well with the measured performance on first samples. This is illustrated in Fig. 4.

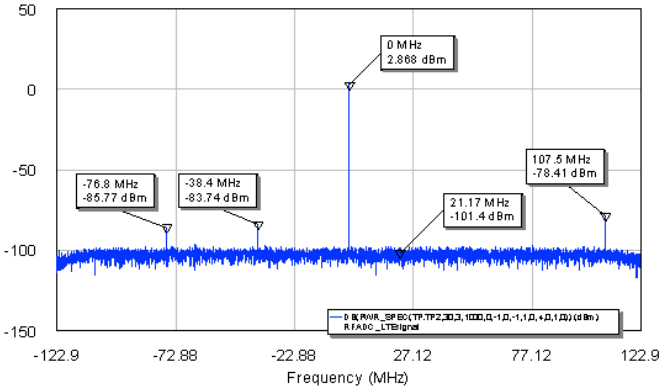

Fig. 4. Model output at digital baseband with all digital impairments and thermal noise included.

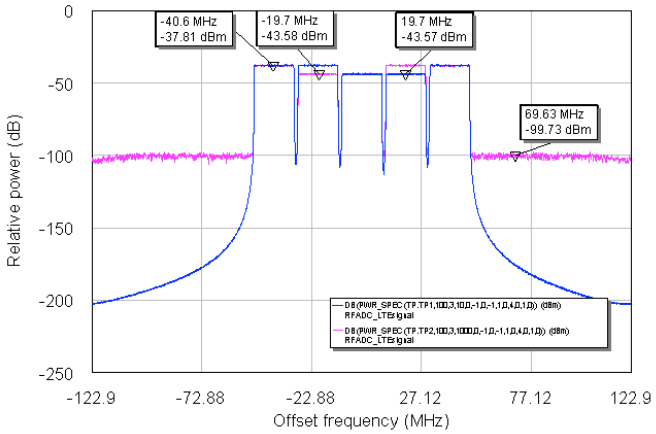

Fig. 5. Comparison of the input signal and the ADC behavioral model output at digital baseband for a 5x20 MHz LTE signal; the carrier frequency is in the 2^{nd} Nyquist zone of the ADC: the output spectrum is 'reversed,' as expected. The input signal is in blue, model output in magenta.

The response of the ADC behavioral model to a modulated signal comprising five adjacent LTE channels of 20 MHz each, sampled at 245.76 MSps, is shown in Fig. 5. This signal is centered at 1860 MHz, and hence is in the second Nyquist zone of the ADC. The model output spectrum is therefore reversed when compared to the original input data in the complex baseband. This can be seen clearly in Fig. 5, as the power in each LTE channel is not identical. The peak-to-average power ratio (PAPR) of this composite signal is about 12 dB, yielding a dynamic range of about 75 dB.

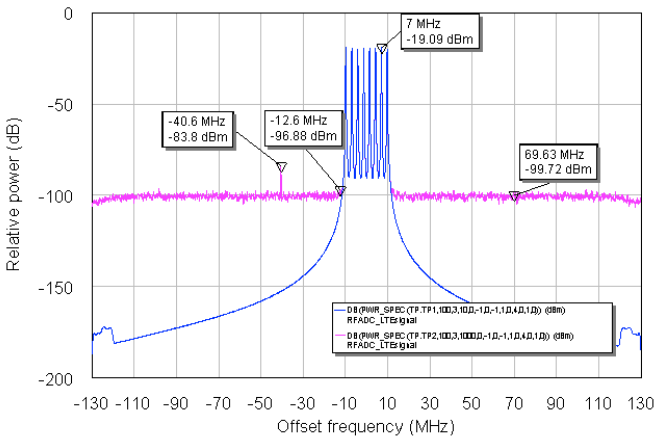

Fig. 6. Comparison of the input signal and the ADC behavioral model output at digital baseband for a 20 MHz BW 8C-GSM/EDGE signal. The input signal is in blue, model output in magenta.

The nonlinearities in the analog front end can be seen using a multi-carrier EDGE signal. The signal has 8 carriers spread uniformly over a 20 MHz bandwidth, and a PAPR of 9.5 dB. The 3^{rd}-order intermodulation products can just be observed (Fig. 6) with a maximum value of -78 dBc, yielding a satisfactory linear dynamic range for MC-GSM/EDGE signals.

VII. Conclusion

A nonlinear behavioral model for a direct RF-to-digital interleaving ADC has been constructed in MATLAB from transistor-level circuit simulation data, and implemented in AWR VSS system simulator. Analog nonlinearities and memory effects, and digital impairments such as voltage offsets and jitter have been included in the model. Testing in VSS shows good predicted performance for a range of wideband wireless signals, consistent with expected performance from the IC process and circuit architecture. The model will be used in the design of receiver system architecture prior to the availability of first silicon.

Acknowledgments

Thanks are due to our colleagues in Maxim, Jim Bales for the analog design, and Wuttichai Lerditsomboon for the analog circuit simulation data, and to Maxim RF Solutions management for sponsoring this modeling work.

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