Zero-IF Radar Signal Processing

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***Abstract*—In this paper, a zero-IF radar architecture is presented. An agile prototyping environment is shown, based on the capabilities of modern instrumentation complemented by COTS components and minimal custom circuitry. Receiver sensitivity improvements based on the oversampling and antipodal modulation techniques are described.**

Keywords—radar; signal processing; zero-IF; oversampling; 0/π modulation

I. INTRODUCTION

In the framework of solid state maritime navigation radars, a cost-effective modular demonstrator operating at S-band has been designed based on available instruments and COTS components. The RF carrier is modulated by an arbitrarily coded sequence. Received echoes are filtered and sampled after base-band down-conversion by a phase-locked vector demodulator. A software radar signal processor is implemented to evaluate multiple signal processing algorithms. Simple digital signal processing techniques are shown to drastically improve the overall receiver performance. Especially in a zero-IF architecture, a notable processing gain can be achieved with minimal hardware and computational requirements.

Preliminary results suggest that coherent, zero-IF, solid state radars may yield an overall data quality comparable to pulsed radar systems, while drastically reducing the unit costs, maintenance needs and power consumption.

II. SYSTEM ARCHITECTURE

A. Concept architecture

The demonstrator architecture is here depicted.

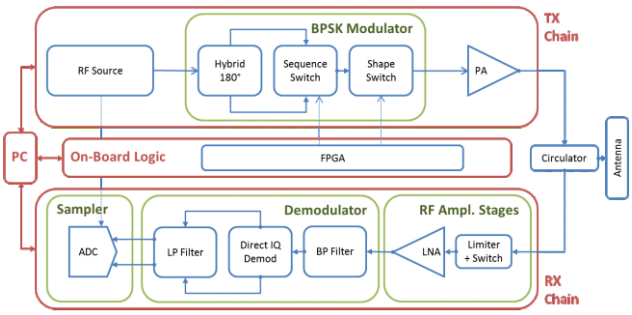

Fig. 1 Concept architecture.

This conceptual block diagram is basically designed to enable two key capabilities: the generation of a custom sequence, transmitter side, and the direct base-band vector demodulation, receiver side. A concept BPSK modulator is described based on a 180 degree hybrid feeding a SP2T switch. The switch is operated from a FPGA to generate the user sequence. The 'shape switch' is intended to blank the RF source in receive mode. A RF power amplifier (up to 200 W at 3 GHz) is available to generate a broad range of output levels.

Following the front-end circulator, receiver protection and transmitter leakage mitigation are attained combining a high power RF limiter followed by an active isolation switch. This limiting circuitry is designed to protect the receiver in case of exceptional events like a full wave reflection from the transmitter (this may happen if the transmitter cable or the antenna get damaged). During normal operations, the switch commutes to the receiver chain by the end of the transmitted sequence. This component has been selected to offer enough transmitter isolation so to avoid saturation up to the last component of the receiver chain. This prevents the generation of harmonics and discharge effects that would otherwise degrade the overall receiver sensitivity.

The received echoes are amplified by a low noise multistage chain (up to 60dB of gain are obtained cascading four shielded amplifiers). Following a 200 MHz band pass filter (providing some interference mitigation), the actual direct conversion and coherent demodulation are performed on a single chip (the direct vector demodulator ADL5380, Analog Devices). This circuitry down-converts the incoming RF signal to the phase and quadrature base-band components. Two low-pass 5th order filters (based on the ADA4857 Op Amps, Analog Devices) operate the anti-alias and noise reduction analog signal conditioning. The filtered (base-band) waveform is then sampled using a dual channel 14 bits ADC card (Gage CS8329, DynamicSignals LLC). Finally, the dual channel data stream is downloaded onto a PC for post processing and permanent storing.

B. Implemented architecture

Even though the above concept block diagram has been initially implemented, a potential to lower the overall demonstrator cost has been noted and has led to the design of a simplified implementation, sketched as in Fig. 2.

Here, some of the capabilities of the available instrumentation have been exploited to embed the modulation blocks within the RF source (Agilent E8267D signal generator

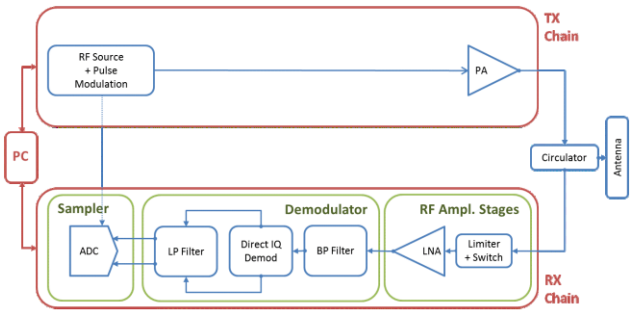

Fig. 2 Implemented architecture.

driving a power amplifier with a gain of 30 dB). In fact, the RF source can be instructed to perform an arbitrary modulation on the CW carrier, and to blank the transmitter at the end of the sequence. Furthermore, the same blanking signal can be conditioned to properly drive the isolation switch. Finally, an RF source trigger and clock reference are available as signal generator outputs to synchronize the ADC card. Signal phase coherency is achieved providing a phase-locked CW carrier from the RF source to the vector demodulator. An in-line memory dump from the ADC card uploads new raw packages on the PC for post-processing and storing.

A real-time hardware sub-system (performing all the raw radar operations) is described comprising the signal generator and the receiver chain up to the ADC card memory banks. Indeed, this approach defines a real-time, FPGA-less rapid prototyping environment, since capabilities and control signals from a signal generator have been found to be sufficient to drive all the necessary real-time blocks. A high level of signal integrity is here achieved since all radar operations are instrument-based and performed in real-time hardware. Higher level signal processing is performed off-line on a regular PC so to rapidly design and verify different processing algorithms.

III. Signal Processing

The ADC memory dump makes digitized samples available for the digital processing stages, here outlined from the received voltages to the range profiles and Doppler maps. Along-range samples (a *scan* in the following) are clipped to cover the desired range and aggregated in logical *frames*. Blocks of frames are clustered together to form a range-time map. The final aggregation of a map yields a *profile* or a range-Doppler map if Doppler processing is applied. To simplify the curves interpretation, the radar antenna has been here replaced by a matched load, so that no actual echoes are received from the environment.

Two key techniques are exploited to digitally improve the receiver performance, based on the zero-IF architecture choice and the digital nature of the demonstrator.

A. 0/π Modulation

Within this waveform aggregation strategy, the pulse polarity is switched at the frame level (from scan to scan) and then digitally compensated at the receiver side. Since the electronics distortion will be independent from the pulse polarity and targets on the scene are preserved (after the polarity compensation), the net effect is a notable reduction of the receiver distortion floor (thus increasing the sensitivity for stationary small targets).

Fig. 3 and 4 highlight the achievable sensitivity improvement comparing the same range-time map and the corresponding profile when the 0/π modulation is switched on and off (all other conditions unchanged, map profile represented in black).

B. Oversampling

The process of sampling a signal at a rate greater than its Nyquist band is referred to as *oversampling*. Apart from relaxing the anti-alias filter constraints, the noise power improvement lies on the fact that the quantization noise power is independent form the signal bandwidth.

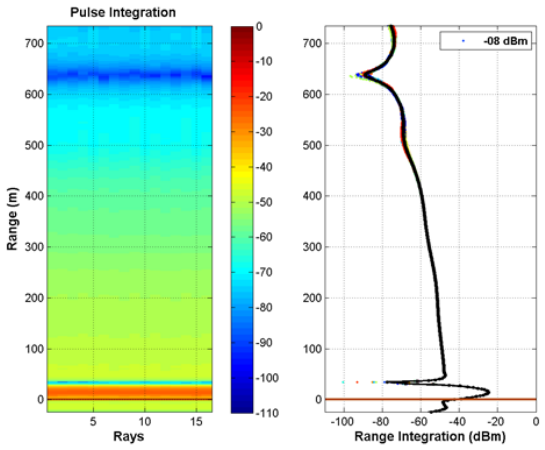

Fig. 3 Sample profile without 0/π modulation (black curve).

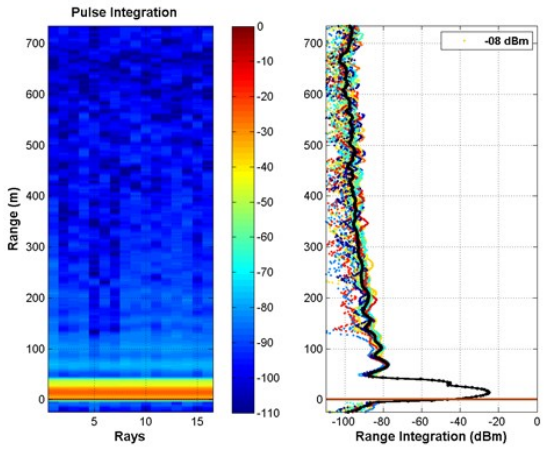

Fig. 4 Sample profile with 0/π modulation.

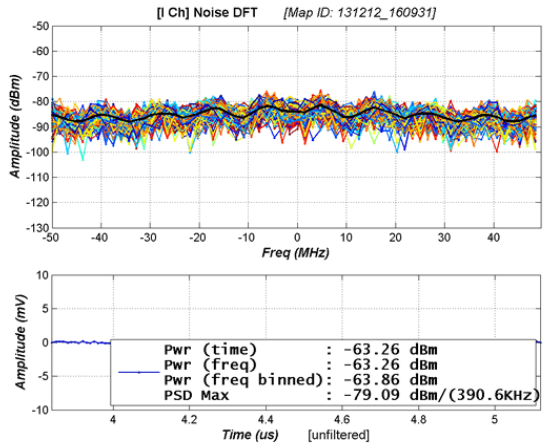

Fig. 5 Noise DFT without processing.

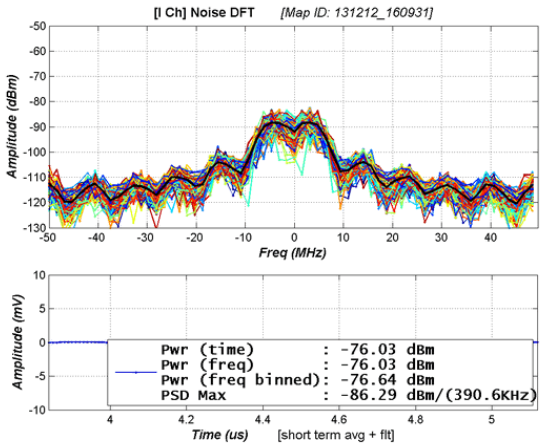

Fig. 6 Noise DFT after oversampling and digital filtering.

The effectiveness of the digital low-pass filtering for noise shaping of an oversampled data stream is exemplified in Fig. 5 and 6.

Here, the noise spectra of the map scans are aggregated (black line) before any processing (Fig. 5) and after the frame level integration plus digital filtering (Fig. 6). Here the base-band waveform (a bandwidth of about 5MHz) is sampled at 100 MSps.

Since the same quantization noise power is spread over a bandwidth extended by an oversampling factor of 10, a nominal noise power reduction of 10 dB is expected after digital filtering (9.8 dB are actually measured). A decimation stage can then lower the data rate by the same oversampling factor without any loss of information,

C. *Overall processing gain*

In Fig. 7, range-time and range-Doppler maps are reported on a 100 dB scale, before applying any processing (internal pulse reflections and pre-trigger data also shown).

Due to the frame level integration, about 3 dB of noise reduction are obtained averaging 2 scans. The averaging is performed after the polarity compensation, as an extra benefit of the antipodal framing technique. Finally, Fig. 8 depicts the same scenario at the end of the processing chain. Given the overall (unfiltered) analog bandwidth at the ADC stage and the residual coherent noise floor, about 10 dBs of further noise reduction are obtained. This sets the overall sensitivity of the receiver chain at about -94 dBm, a sensitivity improvement of about 13 dB.

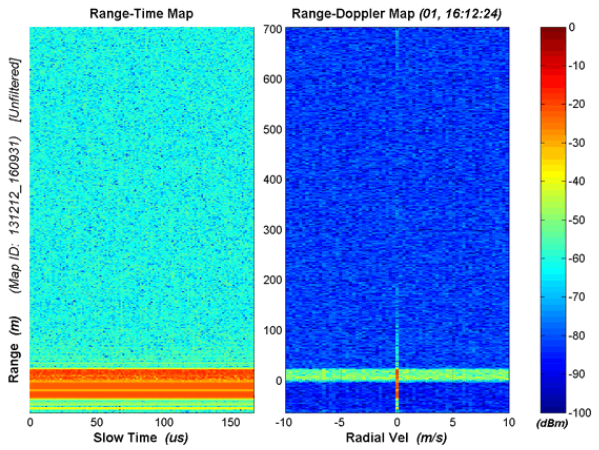

Fig. 7 Range-time and range-Doppler maps at the processing chain input.

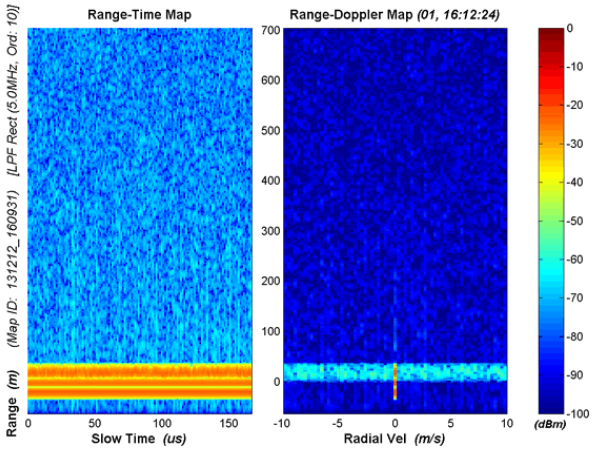

Fig. 8 Same maps at the processing chain output.

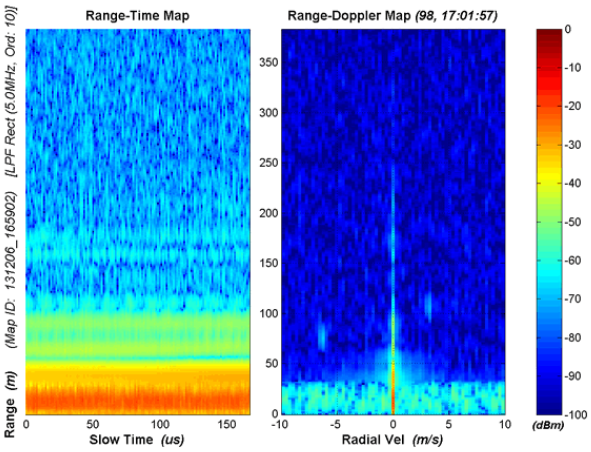

Fig. 9 Experiment scenario at the time-stamp 17:01:57.

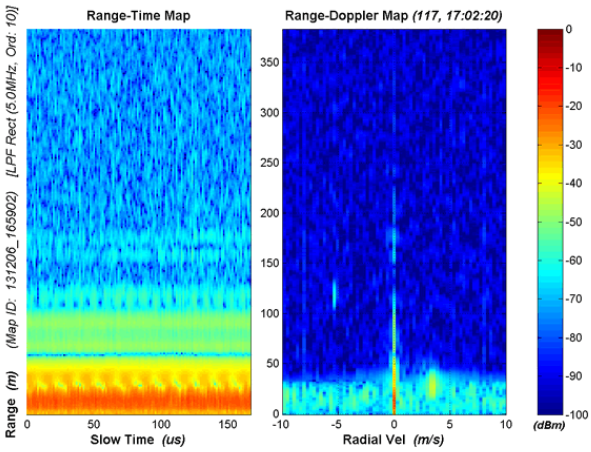

Fig. 10 Experiment scenario at the time-stamp 17:02:20.

IV. An Experimental Case Study: Tracking of Cars along a Road

The adopted signal processing chain is here described by means of a simple experimental case study, the detection of moving cars along a road.

A. Setup

The demonstrator setup follows the architecture here described, based on the Agilent E8267D signal generator driving RF and base-band components and triggering the ADC card.

For this experiment, the RF source was programmed to synthesize a 65536 samples waveform, with bit timespan of 10 ns. Given the geometry constraints (the test road is about 200 meters long), a single 100 ns pulse has been used. This would yield at 3 GHz a maximum Doppler shift corresponding to 38.15 m/s. However, every pair of scans is framed together thus halving the actual PRT and lowering the maximum speed to 19.07 m/s. Very low power is used, since not even 1 Watt is emitted over a 100 ns pulse with a duty cycle of 0.015%. Only 512 samples (a 768 meters range) are actually kept for further processing. Blocks of 128 frames are clustered together to form a range-time map. Given a factor 10 oversampling (100 MSps for a 5 MHz base-band pulse), and the ADC analog bandwidth of about 30 MHz, the anti-alias filters have been here switched off and substituted by their digital low-pass counterparts.

B. Results

Range-time and range-Doppler maps of the experiment are reported. In Fig. 9 a test target is closing (positive Doppler shift), while a second car is opening. The test vehicle is finally getting back to the starting point while another car is opening at a 115 meters range (Fig. 10).

V. Conclusions and Outlook

With this work, a zero-IF radar architecture has been investigated. A methodology for agile prototyping and validation has been presented as well. Indeed, when complemented with inexpensive custom base-band circuitry, the capabilities of modern instrumentation have been proven sufficient to provide all the hardware support needed for proof-of-concept investigations, from the digital post-processing down to the radar signal level.

The key processing stages have been shortly described, highlighting the benefits of the oversampling approach (and related digital noise shaping filters), when backed by simple short term strategies (the two scans $0/\pi$ modulation) able to drastically lower the electronics distortion floor. A simple experiment has been described, exploiting these techniques to detect multiple targets in a low power scenario.

A number of improvements can be investigated given this prototyping platform, including the analysis of more complex short term aggregation patterns, the extended use of hardware differential signals, and the implementation of waveform agile strategies to further exploit the potentials of electronics advancements in the field of solid state coherent radars.

References

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[5] *ADA4857-1: Ultralow Distortion, Low Power, Low Noise, High Speed Op Amp*, Analog Devices, Inc.

[6] *Gage CS8329 Octopus CompuScope 14-Bit, 125MS7s PCI Digitizer Osciloscope Board*, DynamicSignals LLC