An 8.3 nW -72 dBm Event Driven IoE Wake up Receiver RF Front End

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***Abstract*— This work presents an ultra-low power event driven wake-up receiver (WuRx) fabricated in a RF CMOS 130 nm process. The receiver consists of an off-chip lumped element matching network, an envelope detector, a decision circuit capable of detecting sub-mV baseband signal voltages and a clock source consuming 1.3 nW. This receiver has demonstrated a sensitivity of -72 dBm while consuming a total of 8.3 nW from 1 V and 0.65 V sources.**

I. Introduction

Event driven wake-up receivers are a crucial component in emerging remote IoE sensing applications. This has become a major driving force for researchers to develop sensor nodes capable of operation under stringent power consumption limits to the order of several nano-Watts which can remain in a "asleep yet aware" state and switch operation mode upon reception of RF wake-up signals with no need for maintenance over several years [1]. Furthermore, false wake-up events can increase the energy overhead of the node due to temporarily changing operating state. This indicates that very low false alarm rates are required as these events carry a significant energy penalty associated with them.

For event driven wake-up receiver applications, the information transmitted to the receiver can be viewed as a single bit signal that informs the node to wake-up, with data rates ranging from once a minute to once per year depending on application and network activity factor, indicating that total dc power consumption and RF power sensitivity are the critical design requirements. This is significantly different from traditional low power radio receivers in which data rate and energy efficiency are the critical design parameters.

When comparing the received energy sensitvity of square law region receiver circuits it is important to realize that due to the dominant quadratic nonlinearity, output signal power is related to the square of the input signal power. This dominant nonlinearity indictates that the traditional metric of received energy per bit does not scale linearly with respect to RF input power and datarate.

Fortunately square law detector circuits have been used for decades in such disparate fields as Terahertz spectrosophy and photodetectors in fiber optic communications where the most useful receiver sensitivity metric has been found to be "the noise equivalent power" [2] or NEP which is defined to be the input RF power level required to acheive a output SNR of 0dB in a 1 Hertz IF bandwidth. This metric can be found by dividing the output noise voltage of the detector by the open circuit voltage sensitvity of the detector.

This work has extended the state of the art in regards to sub-μW wake-up receivers demonstrating low power and higher sensitivity.

II. Wake-Up Receiver Design

Tight integration between components in the design of a wake-up receiver is crucial to optimal performance. This receiver has been optimized for sub-10nW continuous operation, high RF power sensitivity (<-70 dBm) and very low received energy sensitivity (<30 pJ) with sub pw/$\sqrt{Hz}$ noise equivalent powers.

The system block diagram is shown in Fig. 1. Due to strict dc power requirements, an envelope detector was chosen as the first block in the receiver chain as larger bias currents (>1 μA) are required for amplification at frequencies above 100 MHz. All voltage gain is therefore accomplished passively through the use of an impedance matching network. Examining active CMOS envelope detectors indicates that the noise power of an active detector is inversely proportional to its bias current. Consequently, at very low dc power levels passive rectifiers provide greater sensitivity. The Dickson envelope detector was chosen due to its ability to achieve high RF sensitivity and sufficient noise performance with zero dc power consumption. The output of the rectifier is dc coupled into the preamplifier of a latched comparator which amplifies the offset voltage of the preamplifier using regenerative feedback. The output signal can then either be used directly as a wake-up signal as shown in Fig. 1 or drive a digital correlator which can both decrease false alarm rate and allow discrimination between multiple nodes [4].

A. RF Front end

All voltage gain is accomplished passively through the use of a tapped capacitor impedance matching network which transforms the 50 Ω source impedance into the high impedance at the envelope detector interface, maximizing the input RF voltage without the use of an RF preamplifier. The input RF voltage is limited primarily by three components: the finite Q

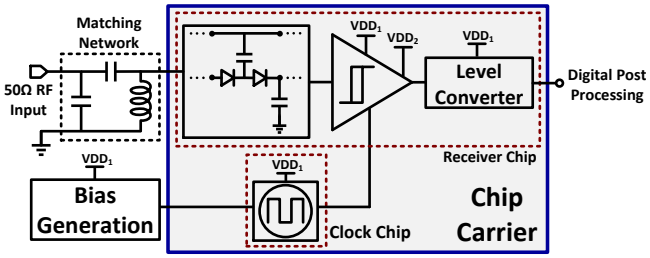

Fig. 1. System level block diagram of the wake-up receiver

of the inductor, the finite real conductance of the rectifier, and dielectric losses into the substrate as shown in Fig. 2. As the high impedance node is shunted with the conductance of the substrate, it is required to use a low-loss dielectric substrate. A high Q (∼150) air-core inductor was used along with a 60 mil Rogers 4350 substrate with dielectric constant of 3.4 to mitigate parasitic losses.

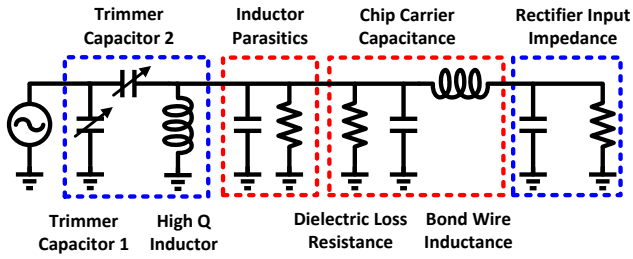

Fig. 2. Matching network model including parasitic elements

The Dickson envelope detector can be modeled as several diode detectors in parallel with respect to the RF input signal, whose baseband output signals are in series. Assuming that the output noise is dominated by the detector device noise, for a given detector noise equivalent bandwidth, output SNR is proportional to $\sqrt{N}$ with N being the number of stages, until the input match starts to degrade. The detector was optimized for high open-circuit voltage sensitivity (OCVS) defined as the ratio of the output dc voltage to the square of the RF input voltage amplitude, and high speed operation. The size of the charging capacitors in the detector is stepped, with the largest capacitors toward the input, as shown in Fig. 3. This minimizes the time constants associated with the later stages of the network, providing faster response time and optimal detector speed.

A 32 Stage zero voltage-threshold, thick gate oxide (ZVTDG) Dickson detector was chosen for both high sensitivity and high speed. The frequency response of the system is primarily determined by the input matching network as the Dickson detector has a broad bandwidth as indicated on the Fig. 6(d).

B. Decision Circuit

The ground referenced comparator architecture shown in Fig. 4 was optimized for both low-power operation and low

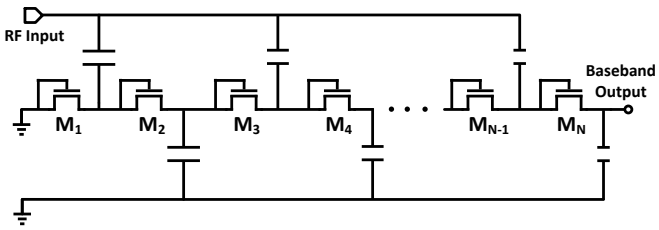

Fig. 3. Utilization of stepped capacitance in Dickson detector reduces the charge time yielding a faster detector with the same OCVS.

decision threshold-voltage. This comparator utilizes current reuse through its preamplifier into its latch which provides the regenerative feedback. The decision voltage of the comparator is determined by a designed mismatch creating an offset voltage between the two legs of the differential amplifier, where the non-signal leg has a digitally controllable width allowing for decision threshold voltage control and compensation. The output of this stage is amplified further and fed into a latch which can then be processed by a digital correlator or used as a wake-up signal. The regenerative latch is clocked such that the comparator amplifies during the negative half of the clock cycle, reducing power consumption and resetting the output of the comparator.

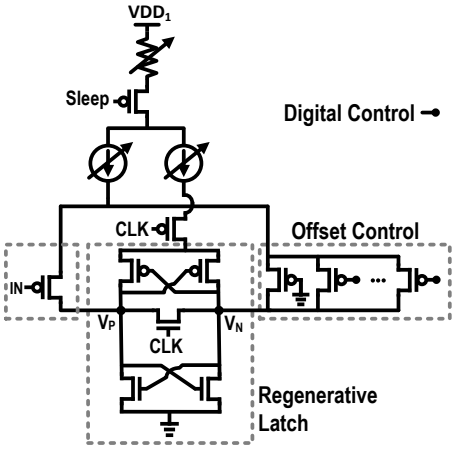

Fig. 4. Schematic of the ground referenced comparator with controllable decision threshold-voltage, capable of detecting sub-mV baseband signals.

C. Clock Source

The system clock was implemented through the use of a 5 stage current-starved ring oscillator as shown in Fig. 5, where the frequency of oscillation was set by two analog controls generated on board by a giga ohm resistive divider that consumes negligible power. The tunable clock can cover a frequency range from 250Hz to 110kHz allowing for a wide range of sample rates from the rectifier. Utilizing a higher clock rate can reduce the total transmitted energy required for a wake-up, but would increase the clock dc power consumption

and degrade the power sensitivity if the detector is not able to fully charge.

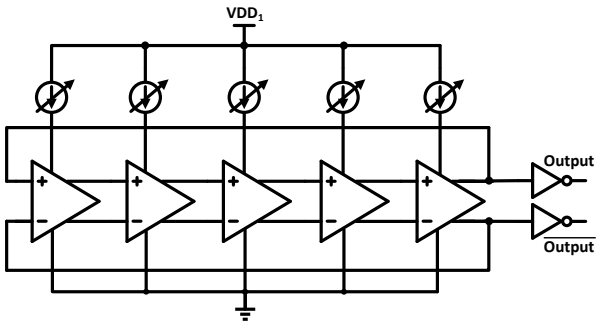

Fig. 5. Schematic of the 5 Stage ring oscillator with broadband tuning range.

D. System level integration

The detector and comparator were dc coupled necessitating a ground referenced comparator design. The system level sensitivity was limited primarily by the minimum comparator decision threshold and both external and internal noise sources. The simulated output device noise of the envelope detector was 1.8 $\mu V/\sqrt{\text{Hz}}$ integrated over a 3 kHz band.

The high impedance zero biased devices used in the detector increase susceptibility to both EMI interferers, and coupling from the in-package clock source. Proper shielding at this node is required to suppress the impact of these parasitic signals.

III. Measurement Results

The system was fabricated in a 130 nm RF CMOS process, where the total active area of the system is 0.12 mm^2. The clock is mounted in package with the main CMOS chip for ease of integration. The total system consumes 8.3 nW of dc power .

A. Block Level Measurements

The envelope detector is characterized in terms of its OCVS and charge time. The envelope detector was first measured using a vector network analyzer with a low input power in order to characterize its input impedance (Fig. 6) and shows a -13 dB match at 162 MHz. The input impedance is measured as a 14.8 kΩ in parallel with a 1.82 pF capacitance. The power sensitivity of the detector circuit without the input matching network is measured to be 28kV/W . The detector bandwidth and sensitivity including the matching network is measured to be 4 MHz and 4.1 mV/nW shown in Fig. 6, resulting in a noise equivalent power (NEP) of 0.44 pW/$\sqrt{Hz}$. The detector charge time (defined by 10% to 90% levels) was measured to be 276 μSec allowing for sub-mSec wake-up pulses. The comparator power was found to be 6.8 nW at a clock rate of 1 kHz. The clock waveform and power versus frequency measurements are given in Fig. 7 showing a linear trend between frequency and power.

Overall system level sensitvity was found to be limited primarily by the minimum input reffered offset of the comparator circuit where a minium decision voltage of 0.5mV was acheived. Reduction of the rectifier noise bandwidth and decreasing the offset voltage of the comparator are likely to yeild an improved power sensitvity but would likely require an integrated offset compensation algorithm and baseband amplifier.

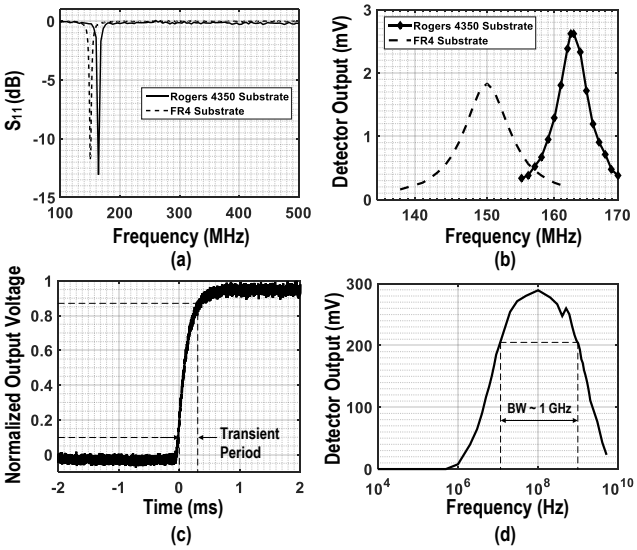

Fig. 6. Measurements of (a) return loss of matched detector, (b) detector output to -62dBm RF tone (c) detector charging curve showing 276 μSec charge time and (d) OCVS of Dickson detector.

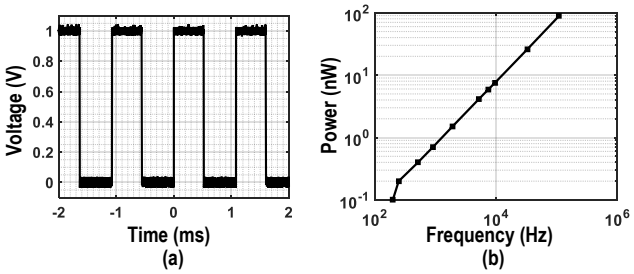

Fig. 7. Measurements of (a) clock waveform and (b) its dc power consumption versus frequency show a low-power clock with a sharp rising edge tunable over a frequency range from 250 Hz to 110 KHz.

B. Receiver Operating Characteristic (ROC) Curves

The digital output of the comparator was charectorized with ROC curves across multiple sensitivity states, uitilzing the receiver without additional baseband filtering. The true positive percentage versus false negative rate at various decision voltage levels known as ROC curves are shown in Fig. 8 where urban interferer data is combined with OOK modulated RF pulses where asynchronous 20 mS pulses were utilized for charectorization. A sensitivity of -64 dBm can be achieved with no false positives out of the comparator over a 12 hour period. At the -68 dBm sensitivity setting, false positive rate at the output of the comparator was found to be less than 0.02 percent at a clock rate of 915 Hz reaching a 100 percent detection rate. At the -69 dBm and -72 dBm sensitivity states it can be seen that the probability of detection drops, and multiple wake-up pulses can be used to improve the true

TABLE I

COMPARISON TO STATE OF THE ART WURX

Metric	This Work	[3]	[4]	[5]
DC Power [nW]	8.3	4.5	236	45,500
VDD [V]	1.0, 0.65	0.4	0.5	0.7
Sensitivity [dBm]	-72	-69	-56.5	-87
Frequency [MHz]	162	113.5	400-2400	924.4
RF Architecture	ED	ED	ED	Mixer
Active Area [mm^2]	0.15	6*	2.25**	1.27
Process	130 nm	180 nm	65 nm	65 nm

* Includes pads. ** Includes energy harvesting PMU and pads.

positive rate. Where the rapid decrease in the true positive rates at -69 and -72 are due to reaching the minimum trip voltage on the comparator.

Table 1 shows a comparison between the state-of-the-art, and Fig. 9 graphically depicts that comparison and shows the die photos of the CMOC chips.

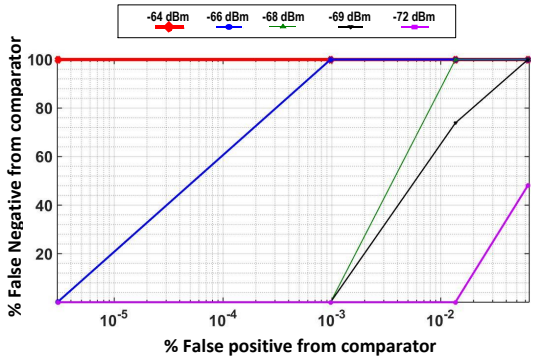

Fig. 8. ROC curves across various RF power levels

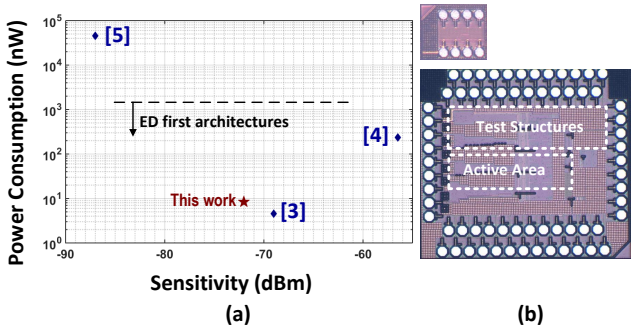

Fig. 9. (a) Comparison of this work to the state-of-the-art and (b) die photos of the clock (upper) and receiver (lower) chips.

IV. CONCLUSIONS

Nano-watt level wake-up receivers based on envelope detector first topologies can reach high RF sensitivities without the use of either RF gain or high power active detectors. Low-power RF design necessitates high system impedances that are not encountered in conventional RF systems, making the system both more sensitive to external noise, as well as increasing the impact of detrimental parasitics at even moderately high RF frequencies. Despite the difficulties of the high impedances introduced, there is much potential in the development of both low-power, and highly sensitive wireless wake-up receivers.

ACKNOWLEDGMENT

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